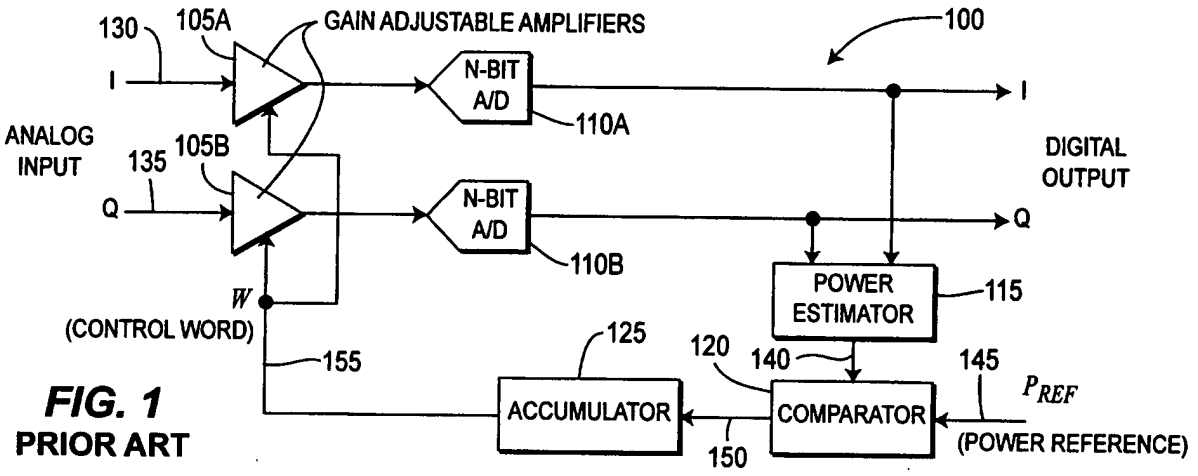

FIG. 1
PRIOR ART

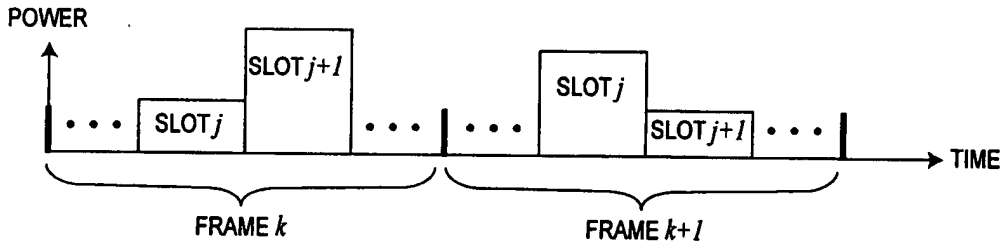

FIG. 2

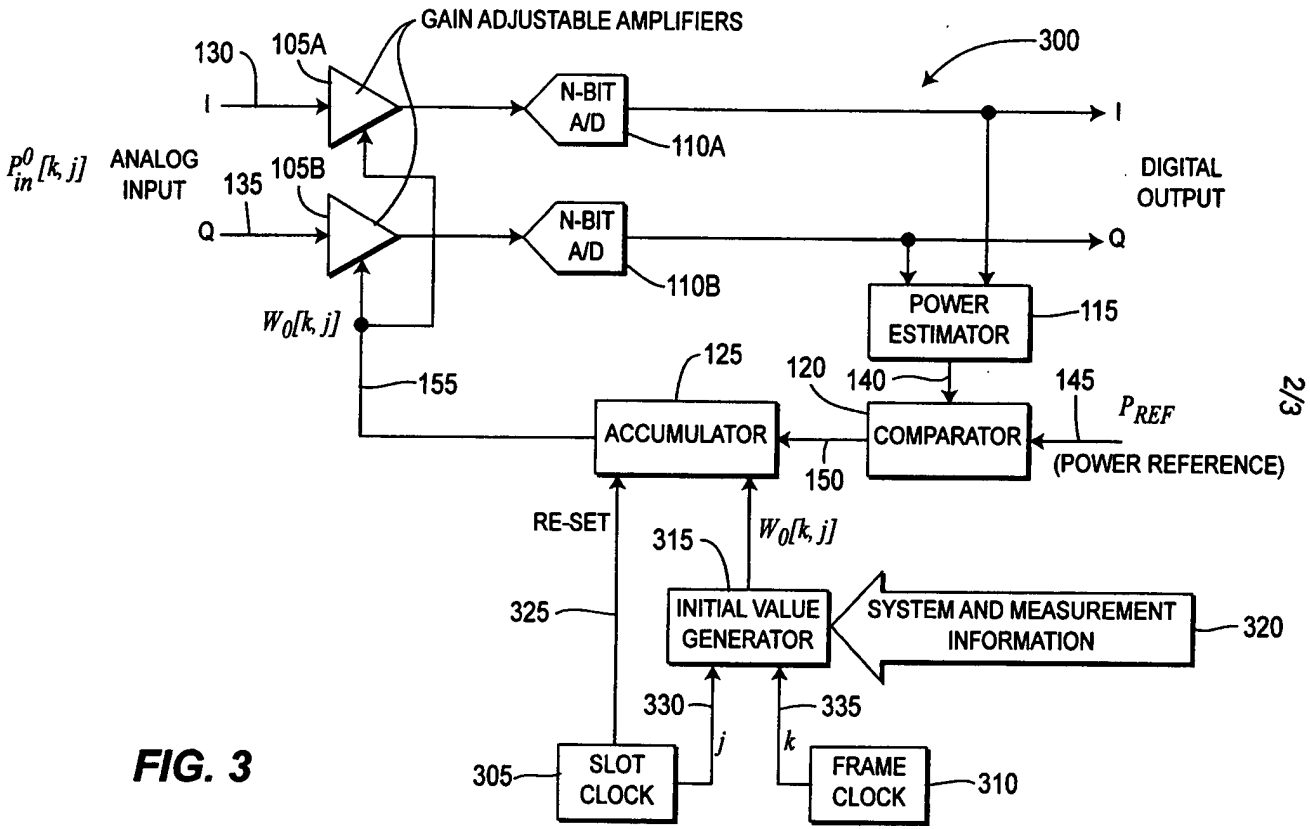
GAIN ADJUSTABLE AMPLIFIERS
130
105A
I
N-BIT A/D
110A
300
I
DIGITAL OUTPUT
$P_{in}^{0}[k,j]$
ANALOG INPUT
135
105B
Q
N-BIT A/D
110B
Q
$W_0[k,j]$
POWER ESTIMATOR
115
155
125
120
140
145
P_{REF}
ACCUMULATOR
COMPARATOR
(POWER REFERENCE)
150
RE-SET
315
$W_0[k,j]$
325
INITIAL VALUE GENERATOR
SYSTEM AND MEASUREMENT INFORMATION
320
330
335
j
k
305
SLOT CLOCK
FRAME CLOCK
310

FIG. 3

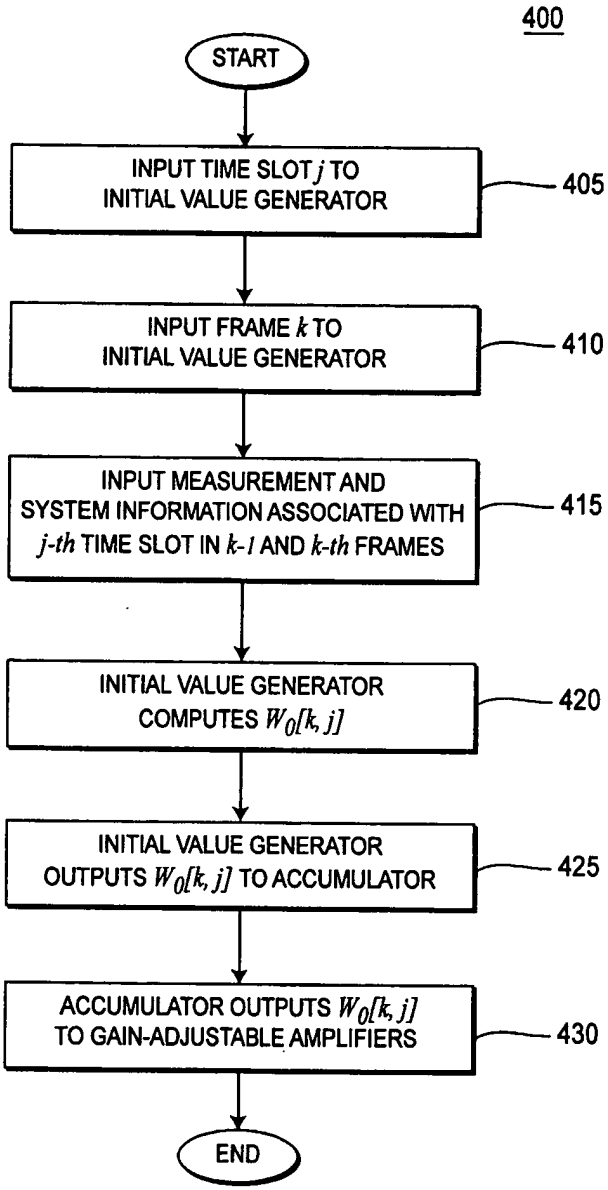
400
START
INPUT TIME SLOT j TO INITIAL VALUE GENERATOR
405
INPUT FRAME k TO INITIAL VALUE GENERATOR
410
INPUT MEASUREMENT AND SYSTEM INFORMATION ASSOCIATED WITH j-th TIME SLOT IN k-1 AND k-th FRAMES
415
INITIAL VALUE GENERATOR COMPUTES $W_0[k, j]$
420
INITIAL VALUE GENERATOR OUTPUTS $W_0[k, j]$ TO ACCUMULATOR
425
ACCUMULATOR OUTPUTS $W_0[k, j]$ TO GAIN-ADJUSTABLE AMPLIFIERS
430
END

FIG. 4